REMARKS

This is a full and timely response to the non-final Office Action mailed by the U.S. Patent and Trademark Office on December 14, 2006. Claims 1-13 are pending in the present application. Claims 4, 5 and 13 are amended to correct typographical errors. Claim 7 is amended to address the rejections under 35 U.S.C. § 112, second paragraph. No new matter is introduced. In view of the foregoing amendments and following remarks, reconsideration and allowance of the present application and claims are respectfully requested.

Drawings

Applicants submit herewith new formal drawings, including the drawing amendments to Figure 5 made in the response filed on December 21, 2005. Applicants respectfully request that the objection to the drawings be withdrawn.

Rejections Under 35 U.S.C. § 112, First Paragraph

Claims 3, 4-6 and 8-13 stand rejected under 35 U.S.C. § 112, First Paragraph, as allegedly failing to comply with the enablement requirement. The Office Action states that the claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 3

Regarding claim 3, the Office Action states "[t]he claimed limitation that 'a predictor and corrector that receive the dithered signal and the reference signal, generating a 'remove pulse' signal; and an output generator, receiving the dithered signal, reference signal, and 'remove pulse' signal, generating a 'clear pulse' signal and the constant frequency output', in claim 3, has not been enabled in the specification because the details of such function is not seen in the description of the preferred embodiment."

With regard to claim 3, Applicants respectfully submit that the block diagram of FIG. 2 together with the flow diagrams of FIGS. 3 and 4, describe the operation of the "simple predict and correct" element 18 and the "output generator" 20 of FIG. 2, respectively.

Specifically, paragraph 0021 of the specification (FIG. 3) states:

> Figure 3 illustrates a flow process diagram 100 for the "simple predictor and corrector" 18 shown in Figure 2. In step 110, the expected_value fractional counter is initialized. In step 120, it is determined whether a fixed reference edge has been received. If no, step 120 is repeated. If yes, in step 130, the expected_value fractional counter is updated. In step 140, it is

determined whether the actual value is greater than the integer of the expected value fractional counter. If no, step 120 is repeated. If yes, in step 150, the "remove pulse" flag is set.

Paragraph 0022 of the specification (FIG. 4) states:

Figure 4 illustrates a flow process diagram 200 for the output generator 20 shown in Figure 2. In step 210, the actual_value integer counter is initialized. In step 220, the output signal is initialized. In step 230, it is determined if there is a high frequency edge. If no, step 230 is repeated until a high frequency edge is detected. If yes, then in step 240, it is determined if remove_pulse flag has been set. If yes, then in step 250, the remove_pulse flag is cleared and the process returns to step 230. If no, then in step 260, the actual_value counter is incremented. In step 270, the output signal is toggled. and the process returns to step 230.

Applicants respectfully submit that FIGS. 2, 3 and 4, together with paragraphs 0020, 0021 and 0022, would enable one having ordinary skill in the art to practice the features of claim 3. Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claim 4

Regarding claim 4, the Office Action states "[t]he claimed limitation that 'a predictor, generating a first output signal indicative of the average number of dithered periods to remove per dithered period', in claim 4, has not been enabled in the specification because the details of such function is not seen in the description of the preferred embodiment."

With regard to claim 4, Applicants respectfully submit that the block diagram of FIG. 6 together with the flow diagram of FIG. 7, describe the operation of the "predictor" 42 of FIG. 6,

Specifically, paragraph 0031 of the specification (FIG. 7) states:

Figure 7 is a flow process diagram 300 corresponding to the predictor 42 shown in Figure 6. In step 310, the average number of high frequency (HF) clocks or dithered clocks is measured for n samples. N may be programmed by the user via the configuration registers. In step 320, the desired number of HF clocks per sample register is determined via the configuration registers. In step 330, the scale factor register value is determined via the configuration registers. In step 340, the difference between the measured clock periods and desired clock periods is determined. This difference is indicative of the average number of HF clocks to remove per sample period. In step 350, the average number of HF clocks to be removed is multiplied by the scale factor register value. This value indicates the average fractional number of HF clocks to remove each HF clock period.

Applicants respectfully submit that FIGS. 6 and 7, together with paragraphs 0030 and 0031, would enable one having ordinary skill in the art to practice the features of claim 4. Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claim 8

Regarding claim 8, the Office Action states "[t]he claimed limitation that 'selecting a desired number of periods in the dithered signal to receive during a sample period of the reference signal; counting the actual number of periods in the dithered signal during the sample period', in claim 8, has not been enabled in the specification for the same reasons. Note the above discussion with regard to claims 3-6."

With regard to claim 8, Applicants respectfully submit that the block diagram of FIG. 6 together with the flow diagrams of FIGS. 7 and 8, describe the operation of the "predictor" 42 and the "corrector" 44 of FIG. 6, respectively.

Specifically, paragraph 0031 of the specification (FIG. 7) states:

> Figure 7 is a flow process diagram 300 corresponding to the predictor 42 shown in Figure 6. In step 310, the average number of high frequency (HF) clocks or dithered clocks is measured for n samples. N may be programmed by the user via the configuration registers. In step 320, the desired number of HF clocks per sample register is determined via the configuration registers. In step 330, the scale factor register value is determined via the configuration registers. In step 340, the difference between the measured clock periods and desired clock periods is determined. This difference is indicative of the average number of HF clocks to remove per sample period. In step 350, the average number of HF clocks to be removed is multiplied by the scale factor register value. This value indicates the average fractional number of HF clocks to remove each HF clock period.

Paragraph 0032 of the specification (FIG. 8) states:

> Figure 8 is a flow process diagram 400 corresponding to the corrector 44 shown in Figure 6. In step 410, the error is measured from the last sample. In step 420, the error is scaled to a fractional error in terms of clocks/clock. In step 430, the scaled error is added to the average fractional number of HF clocks to remove per HF clock. The output represents a fractional number of clocks to remove each clock cycle.

Paragraph 0033 of the specification (referring to the accumulator 46 of FIG. 6) states:

> In operation, the accumulator receives the fractional number of clocks to remove each clock cycle from the corrector. The output generator will remove a clock each time the accumulator output has a value greater than 1, e.g. has overflowed.

Applicants respectfully submit that FIGS. 6, 7 and 8 together with paragraphs 0030, 0031, 0032 and 0033 would enable one having ordinary skill in the art to practice the features of claim 8. Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claim 9

Regarding claim 9, the Office Action states "[t]he claimed limitation that 'determining an average fractional number of dithered periods of the dithered signal to remove each dithered period', in claim 9, has not been enabled in the specification for the same reasons. Note the above discussion with regard to claims 3-6."

With regard to claim 9, Applicants respectfully submit that the block diagram of FIG. 6 together with the flow diagrams of FIGS. 7 and 8, describe the operation of the "predictor" 42 and the "corrector" 44 of FIG. 6, respectively.

Specifically, paragraph 0031 of the specification (FIG. 7) states:

> Figure 7 is a flow process diagram 300 corresponding to the predictor 42 shown in Figure 6. In step 310, the average number of high frequency (HF) clocks or dithered clocks is measured for n samples. N may be programmed by the user via the configuration registers. In step 320, the desired number of HF clocks per sample register is determined via the configuration registers. In step 330, the scale factor register value is determined via the configuration registers. In step 340, the difference between the measured clock periods and desired clock periods is determined. This difference is indicative of the average number of HF clocks to remove per sample period. In step 350, the average number of HF clocks to be removed is multiplied by the scale factor register value. This value indicates the average fractional number of HF clocks to remove each HF clock period.

Paragraph 0032 of the specification (FIG. 8) states:

> Figure 8 is a flow process diagram 400 corresponding to the corrector 44 shown in Figure 6. In step 410, the error is measured from the last sample. In step 420, the error is scaled to a fractional error in terms of clocks/clock. In step 430, the scaled error is added to the average fractional number of HF clocks to remove per HF clock. The output represents a fractional number of clocks to remove each clock cycle.

Paragraph 0033 of the specification (referring to the accumulator 46 of FIG. 6) states:

> In operation, the accumulator receives the fractional number of clocks to remove each clock cycle from the corrector. The output generator will remove a clock each time the accumulator output has a value greater than 1, e.g. has overflowed.

Applicants respectfully submit that FIGS. 6, 7 and 8 together with paragraphs 0030, 0031, 0032 and 0033 would enable one having ordinary skill in the art to practice the features of claim 9. Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claim 13

Regarding claim 13, the Office Action states "[t]he claimed limitation that 'a predictor operative to estimate an average amount of correction per sample; a corrector operative to measure actual error in a previous sample', in claim 13, has not been enabled in the specification for the same reasons. Note the above discussion with regard to claims 3-6."

With regard to claim 13, Applicants respectfully submit that the block diagram of FIG. 6 together with the flow diagrams of FIGS. 7 and 8, describe the operation of the "predictor" 42 and the "corrector" 44 of FIG. 6, respectively.

Specifically, paragraph 0031 of the specification (FIG. 7) states:

> Figure 7 is a flow process diagram 300 corresponding to the predictor 42 shown in Figure 6. In step 310, the average number of high frequency (HF) clocks or dithered clocks is measured for n samples. N may be programmed by the user via the configuration registers. In step 320, the desired number of HF clocks per sample register is determined via the configuration registers. In step 330, the scale factor register value is determined via the configuration registers. In step 340, the difference between the measured clock periods and desired clock periods is determined. This difference is indicative of the average number of HF clocks to remove per sample period. In step 350, the average number of HF clocks to be removed is multiplied by the scale factor register value. This value indicates the average fractional number of HF clocks to remove each HF clock period.

Paragraph 0032 of the specification (FIG. 8) states:

> Figure 8 is a flow process diagram 400 corresponding to the corrector 44 shown in Figure 6. In step 410, the error is measured from the last sample. In step 420, the error is scaled to a fractional error in terms of clocks/clock. In step 430, the scaled error is added to the average fractional number of HF clocks to remove per HF clock. The output represents a fractional number of clocks to remove each clock cycle.

Paragraph 0033 of the specification (referring to the accumulator 46 of FIG. 6) states:

> In operation, the accumulator receives the fractional number of clocks to remove each clock cycle from the corrector. The output generator will remove a clock each time the accumulator output has a value greater than 1, e.g. has overflowed.

Applicants respectfully submit that FIGS. 6, 7 and 8 together with paragraphs 0030, 0031, 0032 and 0033 would enable one having ordinary skill in the art to practice the features of claim 13. Accordingly, Applicants respectfully request that the rejection be withdrawn.

Rejections Under 35 U.S.C. § 112, Second Paragraph

Claim 7 stands rejected under 35 U.S.C. § 112, Second Paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The Office Action states that "[c]laim 7 is rejected... for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP §2172.01. The omitted structural cooperative relationships are the lack of structural and/or functional connections between the dithered signal, the reference signal, data and control signals, and the constant frequency output, as recited in claim 1, and other elements of the frequency synthesizer as recited in claim 7."

Applicants have amended claim 7 to relate the dithered signal, the reference signal and the constant frequency output in claim 7 to the recitations in claim 1.

Regarding the "data and control signals," Applicants respectfully submit that claim 7 defines further the frequency synthesizer of claim 1. The "data and control signals" in claim 1 relate to the configuration registers and, as such, claim 7 does not relate to this feature. Accordingly, Applicants respectfully submit that claim 7 is in compliance with 35 U.S.C. § 112, Second Paragraph, and respectfully request that the rejection be withdrawn.

Rejections Under 35 U.S.C. § 102

Claims 1 and 2 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 5,719,512 to Murayama (hereafter *Murayama*).

A proper rejection of a claim under 35 U.S.C. § 102 requires that a single prior art reference disclose each element of the claim. *See, e.g., W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983). Anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *See, e.g., In re Paulsen,* 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Alternatively, anticipation requires that each and every element of the claimed invention be embodied in a single prior art device or practice. *See, e.g., Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d

1559, 24 USPQ2d 1321 (Fed. Cir. 1992). The test is the same for a process. Anticipation requires identity of the claimed process and a process of the prior art. The claimed process, including each step thereof, must have been described or embodied, either expressly or inherently, in a single reference. *See, e.g., Glaverbel S.A. v. Northlake Mkt'g & Supp., Inc.*, 45 F.3d 1550, 33 USPQ2d 1496 (Fed. Cir. 1995). Those elements must either be inherent or disclosed expressly. *See, e.g., Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir. 1988); *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987). Those elements must also be arranged as in the claim. *See, e.g., Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989); *Carella v. Starlight Archery & Pro Line Co.*, 804 F.2d 135, 231 USPQ 644 (Fed. Cir. 1986). For anticipation, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. *See, e.g., Scripps Clinic & Res. Found. v. Genentech, Inc.*, 927 F.2d 1565, 18 USPQ2d 1001 (Fed. Cir. 1991).

Accordingly, the single prior art reference must properly disclose, teach or suggest each element of the claimed invention.

The Office Action states that:

> Murayama discloses in Fig. 6 a circuit comprising a reference signal (22); a frequency synthesizer (11, 23, 51, 61), receiving a dithered signal (14) and the reference signal, generating a constant frequency output (16); and configuration registers (61, it should be understood that 61 comprises registers since it is latched by the clock signal 62) transceiving data and control signals with the frequency synthesizer.
>
> With regard to claim 2, the circuit further comprises a modulated analog phase lock loop (21, 24, 11, 23, 51), receiving the reference signal (22), generating the dithered signal (14).

Murayama fails to disclose, teach or suggest a circuit as recited in Applicants' claim 1. *Murayama* is directed to a circuit for extracting a color burst sinusoid, both frequency and phase, for an NTSC/PAL/SECAM composite video signal using a reference crystal. The color burst clock signal is extracted from the exact, but intermittent, color burst from the composite video signal. In contrast, with the circuit recited in Applicants' claim 1, a relatively stable clock in the form of the constant frequency output is generated from an arbitrary high frequency input clock in the form of the dithered signal and from a fixed reference clock signal.

Murayama appears to use an incoming frequency controlled clock while in the circuit described in Applicants claim 1, the dithered signal is varying and thus is not an incoming frequency controlled clock signal. The constant frequency output described in Applicants' claim 1 is based upon a fixed frequency reference clock signal as described in the specification and thus this reference signal is a lower fixed frequency reference clock signal as this term is used in Applicants' claim 1. In contrast, the signal 22 in *Murayama* is a burst signal obtained from a composite video signal and is not a reference signal as recited in Applicants claim 1. The reference signal as recited in Applicants claim 1 is a fixed frequency reference having a lower frequency than the high frequency dithered clock signal, with the fixed reference frequency being used to remove clock edges to obtain the desired constant frequency output.

Neither the burst signal applied on the input terminal 22 nor an output from a phase detector 21 generated in response to this burst signal and applied to an input terminal 14, as shown in *Murayama*, is a "dithered" signal as recited in Applicants' claim 1. The term "dithered" is an understood term in the pertinent art and simply calling the burst signal applied on input terminal 22 or the output from the phase detector 21 on input terminal 14 in *Murayama* is not giving the recited "dithered signal" its broadest reasonable interpretation. There simply is neither disclosure, teaching or suggestion in *Murayama* that either of the signals on terminals 22 and 14 is a dithered signal.

Specifically, claim 1 includes at least "a frequency synthesizer, receiving a dithered signal and the reference signal, generating a constant frequency output." Applicants respectfully submit that at least these features are neither disclosed, taught nor suggested by *Murayama*.

Further, it appears that the fsc changing signal output from the television standard discrimination circuit 65 of *Murayama* is used to change the output frequency of the oscillating circuit 11 on connection 16. *Murayama* states:

> [t]he output of the discrimination system 61, i.e., an fsc changing signal, is fed back to the control terminal 17 of the oscillator 11. The television standard discrimination system 61 is provided with an NTSC killer circuit 63 and a PAL killer circuit 64 which both receive the burst signal. The phase detector 51 provides the NTSC killer circuit 63 and the PAL killer circuit 64 with respective suitably phase-controlled color subcarrier signals fsc. The outputs of the killer circuits 63 and 64 are supplied to a television standard discrimination circuit 65 for discriminating the standard of the presently received signal.

See Murayama, col. 9, lines 53-64.

From this it is clear that the system in *Murayama* is merely using information extracted from a composite signal to determine the television standard.

Applicants' respectfully disagree with the statement in the Office Action that "Murayama discloses in Fig. 6 a circuit comprising a reference signal (22); a frequency synthesizer (11, 23, 51, 61), receiving a dithered signal (14) and the reference signal, generating a constant frequency output (16); and configuration registers (61, it should be understood that 61 comprises registers since it is latched by the clock signal 62) transceiving data and control signals with the frequency synthesizer." Applicants respectfully submit that the item 61 in *Murayama* is a "television standard discriminating system" and is not "latched by the clock signal 62" as alleged in the Office action. The element referred to in *Murayama* as a "television standard discriminating circuit 65" is clocked by a clock signal on connection 62. Nowhere does *Murayama* disclose, teach or suggest that the television standard discriminating system 65 is a configuration register.

Accordingly, Applicants respectfully submit that independent claim 1 is allowable over *Murayama*. Further, Applicants respectfully submit that dependent claims 2-7 are allowable for at least the reason that they depend either directly or indirectly from allowable independent claim 1. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988) (Citations omitted).

CONCLUSION

Should the Examiner have any comments regarding the Applicants' response or believe that a teleconference would expedite prosecution of the pending claims, Applicants request that the Examiner telephone Applicants' undersigned attorney.

Respectfully submitted,

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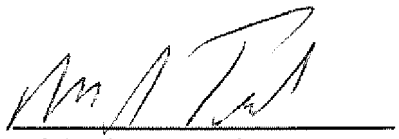
By: 

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